In the Specification

Please amend the paragraph that begins on page 14, line 15 of the specification as follows:

If a physical queue is already allocated for the classification of the new packet, the packet is assigned to an existing physical queue. (Step 440.) However, if there is no physical queue yet allocated for the classification of the new packet, a physical packet is allocated for this purpose in step 445 and the packet is assigned to the new physical queue in step 450. Then, the next packet is arrived, is classified, and so on.

Please amend the paragraph that begins on page 15, line 30 of the specification as follows:

Fig. 6 is a block diagram that illustrates one preferred implementation of the methods described above with reference to Figs 4 and 5. Here, queue selection is done through classification of a packet to a value of Q. The classification mechanism 610 may classify packets can be done, for example, by hashing packet fields, by a lookup table, etc. The resulting Q value (here, a number) indicates the queue in which control information for a packet will be stored.

Please amend the paragraphs that begin on page 15, line 30 of the specification as follows:

Referring now to Fig. 7, a network device 760 suitable for implementing the techniques of the present invention includes a master central processing unit (CPU) [[762]] 761, interfaces 768, and a bus 767 (e.g., a PCI bus). When acting under the control of appropriate software or firmware, the CPU [[762]] 761 may be responsible for implementing specific functions associated with the functions of a desired network device. For example, when configured as an intermediate router, the CPU [[762]] 761 may be responsible for analyzing packets, encapsulating packets, and forwarding packets for transmission to a set-top box. The CPU [[762]] 761 preferably accomplishes all these functions under the

control of software including an operating system (e.g. Windows NT), and any appropriate applications software.

CPU [[762]] 761 may include one or more processors 763 such as a processor from the Motorola family of microprocessors or the MIPS family of microprocessors. In an alternative embodiment, processor 763 is specially designed hardware for controlling the operations of network device 760. In a specific embodiment, a memory [[761]] 762 (such as non-volatile RAM and/or ROM) also forms part of CPU [[762]] 761. However, there are many different ways in which memory could be coupled to the system. Memory block [[761]] 762 may be used for a variety of purposes such as, for example, caching and/or storing data, programming instructions, etc.

The interfaces 768 are typically provided as interface cards (sometimes referred to as "line cards") 770. Generally, they control the sending and receiving of data packets over the network and sometimes support other peripherals used with the network device 760. Among the interfaces that may be provided are Ethernet interfaces, frame relay interfaces, cable interfaces, DSL interfaces, token ring interfaces, and the like. In addition, various very high-speed interfaces may be provided, such as fast Ethernet interfaces, Gigabit Ethernet interfaces, ATM interfaces, HSSI interfaces, POS interfaces, FDDI interfaces, ASI interfaces, DHEI interfaces and the like. Generally, these interfaces may include ports 769 appropriate for communication with the appropriate media. In some cases, they may also include an independent processor and, in some instances, volatile RAM. The independent processors may control such communications intensive tasks as packet switching, media control and management. By providing separate processors for the communications intensive tasks, these interfaces allow the master microprocessor [[762]] 761 to efficiently perform routing computations, network diagnostics, security functions, etc.